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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/762,863
Filing Date: January 22, 2004
Appellant(s): JACOBS ET AL.

Thomas H. Ham
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/25/2010 appealing from the Office action mailed 10/26/2009.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 30-32 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 4,251,862 ("Murayama").

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

4,251,862	Murayama	2-1981

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 30-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Murayama (US 4251862).

3. Consider claim 30, Murayama discloses of a first instruction (Figure 2A, instruction k) including a format field (Figure 2, bit field 101) that specifies an instruction compression format (col. 2, lines 56-63; when the bit 101 is a "0", field 102 is an ordinary control field, and when the bit 101 is a "1", field 102 is used to address the sub-control memory. The bit field 101 of Figure 2 determines whether the following instruction (of a variable number of bits, as noted in col. 1, lines 61-62) is of a shorter length (i.e. if the following instruction does not need to read from the sub-control memory) or is of a longer length (i.e. if the following instruction does need to read from the sub-control memory). In other words, the bit field determines whether the following instruction is compressed in a format to fit solely in the main control memory); and a second instruction, following the first instruction (Figure 2A, instruction k+1), that is compressed according to the format field in the first instruction (col. 5, lines 36-42, where, therefore, a microinstruction read out of the main control memory 1 includes a "1" bit 101 instructing the use of the sub-control memory, then the succeeding microinstruction is executed in the form of a large bit length comprising data read out of the main control memory 1 and data read out of the sub-control memory 11. The bit field 101 of Figure 2 determines whether the following instruction (of a variable number of bits, as noted in col. 1, lines 61-62) is of a shorter length (i.e. if the following

instruction does not need to read from the sub-control memory) or is of a longer length (i.e. if the following instruction does need to read from the sub-control memory). In other words, the bit field determines whether the following instruction is compressed in a format to fit solely in the main control memory).

4. Consider claim 31, Murayama discloses that the second instruction includes a compressed operation, the compressed operation being compressed according to the first format field (col. 5, lines 36-42, where, therefore, a microinstruction read out of the main control memory 1 includes a "1" bit 101 instructing the use of the sub-control memory, then the succeeding microinstruction is executed in the form of a large bit length comprising data read out of the main control memory 1 and data read out of the sub-control memory 11. The bit field 101 of Figure 2 determines whether the following instruction (of a variable number of bits, as noted in col. 1, lines 61-62) is of a shorter length (i.e. if the following instruction does not need to read from the sub-control memory) or is of a longer length (i.e. if the following instruction does need to read from the sub-control memory). In other words, the bit field determines whether the following instruction is compressed in a format to fit solely in the main control memory. The operation is embodied by the bits of the instruction that are not directed toward whether the following instruction accesses the sub-control memory).

5. Consider claim 32, Murayama discloses the second instruction includes a second format field that specifies a compression of an operation in a third instruction (Figure 2A,

for example, instruction K+1 also contains a format field 101 which is used in an analogous fashion).

(10) Response to Argument

6. Appellant first summarizes his position that the cited reference of Murayama does not teach the claimed limitations of claim 30 on page 4 of the appeal brief. Appellant then reproduces examiner's rejection in the previous office action from pages 4-5, and summarizes the implementation details of Murayama from pages 5-6.

7. Appellant then argues on page 6 of the appeal brief that the main microinstructions in the main control memory 1, including the microinstruction k+1, are described in Murayama as being merely stored in the main control memory 1, not compressed into the main control memory 1. Appellant stresses that there no mention of anything related to “compression” in Murayama, and no mention of compressed instructions or microinstructions or any compressed data. Appellant also cites a definition of the term “data compression”. In view of these arguments, Appellant concludes that Murayama does not disclose of “a first instruction including a format field that specifies an instruction compression format” and “a second instruction, following the first instruction, that is compressed according to the format field in the first instruction”.

However, examiner first notes that there is no requirement that a prior art reference must use the exact language of the instant claim language in order to teach

the claim language. Therefore, the fact that Murayama may not disclose of the explicit language "compression" or "compressed instructions" or "compressed microinstructions" or "compressed data" does not preclude Murayama from nevertheless teaching the claim language. Examiner will now explain how Murayama, despite not using identical language as that of the instant claim, nevertheless teaches the claimed limitations.

8. To determine whether Murayama teaches the claimed limitations, particularly the limitations "compression" and "compressed," it is helpful to not only look at the actual implementation details but also the context of the implementation.

First, consider the "Background of the Invention" section of Murayama (Murayama, col. 1, lines 10-36). Before Murayama's improvement, each word of a control memory was read out and processed as a single microinstruction (Murayama, col. 1, lines 26-28). In a parallel horizontal-type microinstruction system, a microinstruction will have a larger number of bits (Murayama, col. 1, lines 29-32). A larger number of bits consequently cause the width of the control memory to likewise increase in order to hold the microinstruction (Murayama, col. 1, lines 32-33). The increase in width of the control memory causes the control memory to become more expensive (Murayama, col. 1, lines 33-34).

Next, consider the "Summary of the Invention" section of Murayama (Murayama, col. 1, lines 39-62). Murayama recognizes that in the aforementioned parallel horizontal-type microinstruction system, some of the respective fields or bit blocks of a microinstruction are supposed to be used less frequently than when data is not

processed in parallel (Murayama, col. 1, lines 44-48). Consequently, Murayama's invention entails storing usually necessary fields in a main control memory and storing usually unnecessary fields in a sub-control memory (Murayama, col. 1, lines 49-55). Usually, the usually necessary fields of a microinstruction are read out from the main control memory (Murayama, col. 1, lines 55-56). However, it is when the data thus read out includes an instruction to use the sub-control memory that the fields of a microinstruction stored in the sub-control memory is also read out (Murayama, col. 1, lines 57-60).

Examiner will now put the "Background of the Invention" and the "Summary of the Invention" section in context with each other. Murayama recognizes that some particular microinstructions may have fields which are unnecessary. Nevertheless, these unnecessary fields still take up memory space in the prior art system, wherein each word of a control memory constitutes a microinstruction even if fields within that particular microinstruction are unnecessary. To improve this system, Murayama determines which instructions do require fields from the usually unnecessary field group for execution, and moves these fields to the sub-control memory. Murayama's system makes it possible to execute a microinstruction constituted by a variable number of bits (Murayama, col. 1, lines 60-62), leading to high versatility and at low cost (Murayama, col. 6, lines 2-4). In other words, Murayama's system does not mandate each microinstruction to be the same number of bits regardless of whether certain fields in the microinstructions are unnecessary; rather; a microinstruction in Murayama's system

can be a smaller number of bits if certain fields of that microinstructions are unnecessary.

To briefly correlate the above general explanation of Murayama's system to specific implementation details, consider Figures 2A and 2B. Each microinstruction (e.g. instruction k) in the main control memory 1 contains a bit field 101 which determines whether the following microinstruction (e.g. instruction k+1) comprises usually unnecessary fields to be sent alongside the usually necessary fields in the main control memory 1 to the processing unit 10.

9. In view of the above explanation of both the context of the Murayama invention and its specific implementation details, the specific claim limitations that Appellant is arguing will now be considered.

The first argued limitation is "a first instruction including a format field that specifies an instruction compression format." Examiner has correlated "a first instruction" to instruction k of Figure 2A, though any instruction would suffice, and has correlated the format field to the bit field 101 of Figure 2. Appellant argues that this bit field 101 does not specify an instruction compression format. However, as explained above, the bit field 101 of Figure 2 determines whether the following instruction (of a variable number of bits, as noted in col. 1, lines 61-62) is of a shorter length (i.e. if the following instruction does not necessitate a usually unnecessary field and thus does not need to read from the sub-control memory) or is of a longer length (i.e. if the following instruction necessitates a usually unnecessary field and thus does need to read from

the sub-control memory). In other words, the bit field determines whether the following instruction is compressed in a format to fit solely in the main control memory. Consequently, it would be reasonable to say that the bit field is a format field that specifies an instruction compression format. In fact, the definition Appellant has attributed to "compression" (page 6, third paragraph of the appeal brief) of "[t]he technique of reducing the number of binary digits required to represent data" correlates to Murayama's technique of reducing the number of binary digits required to represent a microinstruction by forgoing the explicit storing of unnecessary fields that are part of the usually unnecessary field group. Examiner further notes that the applicant uses the term "compression" in the instant specification in an analogous context as the Murayama reference. For example, see page 3 (of the specification filed 5/24/2004), lines 9-11, which correlates compression to the elimination of unused operations in an instruction word.

The second argued limitation is "a second instruction, following the first instruction, that is compressed according to the format field in the first instruction." In further view of the citations of the previous paragraph regarding the first argued limitation, examiner has correlated "a second instruction" to instruction k+1 of Figure 2A which follows the first instruction as shown. Appellant argues that this second instruction is not compressed according to the format field in the first instruction. However, as explained above, the bit field 101 of Figure 2 determines whether the following instruction (of a variable number of bits, as noted in col. 1, lines 61-62) is of a shorter length (i.e. if the following instruction does not necessitate a usually

unnecessary field and thus does not need to read from the sub-control memory) or is of a longer length (i.e. if the following instruction necessitates a usually unnecessary field and thus does need to read from the sub-control memory). In other words, the bit field determines whether the following instruction is compressed in a format to fit solely in the main control memory. Consequently, it would be reasonable to say both that the second instruction is compressed, and that this compression is indicated by the bit field 101. Again, examiner notes that the definition Appellant has attributed to "compression" (page 6, third paragraph of the appeal brief) of "[t]he technique of reducing the number of binary digits required to represent data" correlates to Murayama's technique of reducing the number of binary digits required to represent a microinstruction by forgoing the explicit storing of unnecessary fields that are part of the usually unnecessary field group. Again, examiner further notes that the applicant uses the term "compression" in the instant specification in an analogous context as the Murayama reference. For example, see page 3 (of the specification filed 5/24/2004), lines 9-11, which correlates compression to the elimination of unused operations in an instruction word.

10. Examiner will now revisit Appellant's specific arguments.

11. Appellant argues on page 6 of the appeal brief that the main microinstructions in the main control memory 1, including the microinstruction k+1, are described in Murayama as being merely stored in the main control memory 1, not compressed into the main control memory 1.

However, as previously noted, there is no requirement that a prior art reference must use the exact language of the instant claim language in order to teach the claim language. Therefore, while Murayama may not explicitly use the "compressed" language, examiner has provided a detailed analysis above as to how Murayama nevertheless discloses of an instruction that is compressed into the main control memory.

12. Appellant stresses on page 6 of the appeal brief that there no mention of anything related to “compression” in Murayama, and no mention of compressed instructions or microinstructions or any compressed data.

However, examiner first notes that there is no requirement that a prior art reference must use the exact language of the instant claim language in order to teach the claim language. Therefore, the fact that Murayama may not disclose of the explicit language “compression” or “compressed instructions” or “compressed microinstructions” or “compressed data” does not preclude Murayama from nevertheless teaching the claim language. Examiner has provided a detailed analysis above as to how Murayama nevertheless discloses of an instruction that is compressed into the main control memory.

13. Examiner has explained in detail above how Murayama teaches the claimed limitations, despite Murayama not using the explicit terminology of the instant claims. Consequently, examiner maintains his belief that the pending rejection is valid.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Keith Vicary/

Examiner, Art Unit 2183

Conferees:

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117